

IN THE SPECIFICATION:

Please amend the Specification as follows:

Please substitute the paragraph beginning at page 8, line 11 and ending at page 8, line 11 with the following:

B1
--CPU 200 is connected by address, control, and data busses 202 to a memory controller and peripheral component interconnect (PCI) bus bridge 204 which is coupled to system memory 206. An integrated drive electronics (IDE) device controller 220, and a PCI bus to Industry Standard Architecture (ISA) bus bridge 212 are connected to PCI bus bridge 204 utilizing PCI bus 208. IDE controller 220 provides for the attachment of IDE compatible storage devices, such as a removable hard disk drive 222. PCI/ISA bridge 212 provides an interface between PCI bus 208 and an optional feature or expansion bus such as the ISA bus 214. PCI/ISA bridge 212 includes power management logic. PCI/ISA bridge 212 is supplied power from battery 244 to prevent loss of configuration data stored in CMOS 213.--

Please substitute the paragraph beginning at page 10, line 26 and ending at page 10, line 26 with the following:

B2
--Figure 3 illustrates a high level flow chart which depicts establishing and storing a master key pair in protected storage in a data processing system in accordance with the method and system of the present invention. The process starts as depicted at block 300 and thereafter passes to block 302 which illustrates establishing a master key pair for data processing system 30 (see Figure 1). Next, block 304 depicts the storage of the master public key and master private key in protected storage 262 (see Figure 2) which is a one-time writable, protected storage. The process then terminates as illustrated at block 306.--